Abstract of the Disclosure

An impedance adjustment system comprising current source, a first series and a second series connected string of predetermined number of resistors, a first and second switch network, a first , second and third logic circuit and a comparator. By applying the principles of the present invention, embodiments can be made in which variations in a Silicide block of resistors used to terminate a signal line are "tuned out" to get a more precise termination impedance. Embodiments may be made that hold the termination impedance substantially constant over time by continually adjusting in response to variations in process, temperature and supply voltage. IDDQ requirements can be met by latching, by double buffering, the outputs of comparators providing an encoded resistor network setting for the termination impedance, and then powering down the circuit. Embodiments of the present invention avoid the use of trims and fuses, thus reducing fabrication cost. Finally, embodiments of the present invention may be made that do not require a clock.